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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,190	09/16/2003	Yervant Zorian	4640P019	3960

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,190	ZORIAN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application filed 9/16/2003. Claims 1-30 are presently under examination and still pending in the Application.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "A method and apparatus for a command based BIST for testing memories".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11, 15, 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3, 5, 20, 23 recite the limitation "the processor loads a command containing representations of a march element and data via the serial bus", which renders the claims indefinite, because the expression "representations of a march element" fails to clearly define the march element with respect to the command. It is unclear if the "March" element and data is part of the command.

Claims 6,15, 21 similarly recite the phrase "representation" "representing", which renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention.

Claim 6 recite the limitation "may be", which renders the claim indefinite, because it is unclear whether the limitations following the phrase "may be" are part of the claimed invention.

Claim 11 recites the limitation " that string", which renders the claim indefinite because there is insufficient antecedent basis for this limitation in the claim.

Claims 25, 28, recites the limitation "communicating the compressed information in a serial manner to logic bounding the memory", which renders the claim indefinite because the phrase "in a serial manner" fails to positively identify the communication of the compressed information.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9-11, 25, 26, 28 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by White et al. (US Patent No. 7,007,211) filed: October 4, 2002.

Regarding independent Claim 1, White discloses an apparatus 10, Figures 1-3, comprising:

Two or more memories (20a...20n), wherein each memory 20 has an intelligence wrapper (comprising a Built-in self-tester (BIST) 22, a repair register 24) bounding the corresponding memory.

A host processor coupled to remote processor interface (RPI) 50, which initiates a Built In Self Test for the memories (20a...20n) through a serial bus situated between a central controller 30 and the remote processor interface (RPI) 50.

The host processor loads a command containing "march" element and data via the serial bus, as described in a flowchart of Figure 5, which illustrates a method for testing memories 20 of device 10 used in a circuit system, which tests memories 20 and provides a notification if memories 20 fail.

In view of the 112, second paragraph rejection with respect to claimed feature "representations of a "March" element, the Examiner interprets the feature as "loading a pattern". Each (BIST) 22 includes a state machine 58, which cycles through rows 21 of memory 20 to load a pattern. The pattern may comprise, for example, all zeros, all ones, or a checkerboard. Address tracker 60 tracks the address of the row 21 of memory 20 that is being tested.

Regarding Claims 2-6, White discloses a method, Figure 5, beginning at step 200, where the host processor of the circuit system resets a circuit system. The host

processor initiates a test of memories 20 at step 202. The host processor may initiate the test by accessing device 10 through remote processor interface 50. Built-in self-testers 22 generate repair records at step 204. The repair records are collected using scan bus 40 at step 206. Central controller generates a repair signature from the repair records at step 208.

Regarding Claim 7, White discloses the memories (20a...20n) share the same host processor through the central controller 30.

Regarding Claims 9, White discloses, Figure 2, a block diagram of the built-in self-tester 22 of Figure 1. The built-in self-tester 22 supplies a series of patterns, for example, checker board patterns, to memory 20 and compares the output of memory 20 against a set of expected responses to identify any defective rows 21b. Built-in self-tester 22 records the address of a defective row 21b in a repair record, and repairs the defective row 21b by substituting a spare row 23 for the defective row 21b.

Regarding Claims 10, 11, in view of the 112, second paragraph rejection with respect to claimed limitation recited in claim 10, the Examiner interprets the limitation as comprising a pattern including all zeros, all ones, or a checkerboard, and tracking the address of the row 21 of memory 20 that is being tested. In reference to the term "that string", White discloses loading a pattern with corresponds to a series of bits.

Regarding independent Claims 25, 28, a method and apparatus, 10, Figures 1-3, comprising:

Compressing information by serially loading a pattern using a Built In Self Test 22 for the memories (20a...20n) through a serial bus situated between a central controller

30 and the remote processor interface (RPI) 50, wherein the memories (20a...20n) are embedded on a circuit chip 10.

Communicating the compressed information (serially loaded pattern) to a the BIST 22 bounding the memories (20a...20n).

Regarding Claims 26, 29, expanding the compressed information (serially loaded pattern) to perform the self-test on memories (20a...20n).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 12-24, 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. (US Patent No. 7,007,211) in view of Hayashi et al. (US Patent No. 6,779,144).

Regarding independent Claims 12, 21, White substantially discloses an apparatus 10, Figures 1-3, comprising:

Two or more memories (20a...20n), wherein each memory 20 has an intelligence wrapper (comprising a Built-in self-tester (BIST) 22, a repair register 24) bounding the corresponding memory.

A host processor coupled to remote processor interface (RPI) 50, which initiates a Built In Self Test for the memories (20a...20n) through a serial bus situated between a central controller 30 and the remote processor interface (RPI) 50.

The host processor loads a command containing "march" element and data via the serial bus, as described in a flowchart of Figure 5, which illustrates a method for testing memories 20 of device 10 used in a circuit system, which tests memories 20 and provides a notification if memories 20 fail.

In view of the 112, second paragraph rejection with respect to claimed feature "representations of a "March" element, the Examiner interprets the feature as "loading a pattern". Each (BIST) 22 includes a state machine 58, which cycles through rows 21 of memory 20 to load a pattern. The pattern may comprise, for example, all zeros, all ones, or a checkerboard. Address tracker 60 tracks the address of the row 21 of memory 20 that is being tested.

Regarding Claims 8, 12, 13, 21, 27, 30, White does not explicitly disclose, the logic contained in the intelligence wrapper operating at a clock speed asynchronous to a clock speed of the processor.

In analogous art, Hayashi discloses an apparatus and method of testing a large-scale integrated (LSI) circuit device operated by a high-frequency clock signal, Figure 9. The LSI can be tested by the control operation (setting the BIST circuit for the test and reading the test result) at low frequencies using a tester having a low capability as compared with the operating speed of the LSI to be tested by providing control means operated "asynchronous" with the clock, i.e. means for "slow control operation". With

this tester capability, the data are often input and output at about the resonance frequency of the power circuit.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the method as taught by Hayashi with the method disclosed by White, by using a high-frequency clock at the operating speed of the LSI and a clock with low frequencies using a tester. A person skilled in the art would have been motivated to do so, since the test circuit and the test method according to Hayashi can fully exhibit the performance as a test circuit without operating at a lower frequency by avoiding the resonance frequency band, and therefore the test time can be shortened effectively.

Regarding Claims 14-16, White discloses, Figure 2, a block diagram of the built-in self-tester 22 of Figure 1. The built-in self-tester 22 supplies a series of patterns, for example, checker board patterns, to memory 20 and compares the output of memory 20 against a set of expected responses to identify any defective rows 21b. Built-in self-tester 22 records the address of a defective row 21b in a repair record, and repairs the defective row 21b by substituting a spare row 23 for the defective row 21b.

Regarding Claims 17-20, 22-24, White discloses a method, Figure 5, beginning at step 200, where a circuit system is reset by the host processor, which initiates a test of memories 20 at step 202. The host processor may initiate the test by accessing device 10 through remote processor interface 50. Built-in self-testers 22 generate repair records at step 204. The repair records are collected using scan bus 40 at step 206. Central controller generates a repair signature from the repair records at step 208.

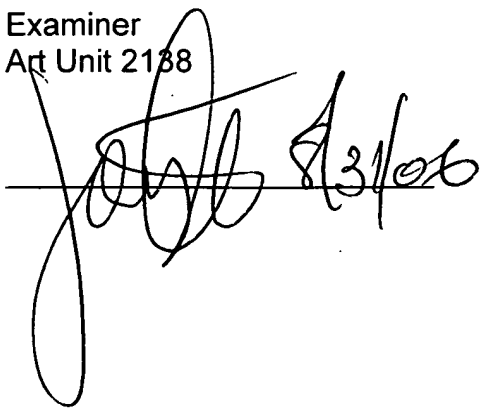
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



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Office Action: Non-Final Rejection